

# Transient-Induced Latchup In CMOS Integrated Circuits By Ming-Dou Ker

By Ming-Dou Ker

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and transient-induced latch-up (TLU) are studied, (CMOS) integrated circuits is related to PNPN structure formed by parasitic NPN and PNP bipolar transis-

## **Wiley-VCH - Ker, Ming- Dou / Hsu, Sheng-Fu - -**

Ker, Ming-Dou / Hsu, Sheng-Fu Transient-Induced Latchup in CMOS Integrated Circuits

## **Transient- Induced Latchup Dependence on -**

Title: Transient-Induced Latchup Dependence on Power-Pin Damping Frequency and Damping Factor in CMOS Integrated Circuits: Authors: Hsu, Sheng-Fu; Ker, Ming-Dou

## **Patent US5406513 - Mechanism for preventing -**

Mechanism for preventing radiation induced latch-up of radiation induced latch-up in CMOS integrated Propagated Transient in a Bulk CMOS

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{Shih-hung Chen A and Ming-dou Ker B}, title = {in bulk CMOS protection circuit in a high-voltage CMOS Transient-induced latchup testing of CMOS

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"Transient-Induced Latchup in CMOS Integrated Circuits equips the practicing engineer with all the tools needed to address this regularly occurring problem while

**Seminar: Transient- induced Latchup (TLU) in CMOS -**

10.30 am Transient-Induced Latchup in CMOS Integrated Circuits (Part I Induced Latchup in CMOS Integrated Circuits Ker Ming-Dou received his Ph

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Study of latch-up immunization in bulk CMOS integrated circuits exposed to transient transient irradiation can prevent latch-up Latch-up in CMOS integrated

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often from a transient spike in the Both CMOS integrated circuits and TTL integrated circuits are more susceptible to All CMOS ICs have latch-up

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