

# Transient-Induced Latchup In CMOS Integrated Circuits By Ming-Dou Ker

By Ming-Dou Ker

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OF SUBMICRON CMOS LATCHUP WITH A PHYSICAL CRITERION MING-DOU KER and CHUNG-YU WU Integrated a physical criterion for transient latchup which is

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and transient-induced latch-up (TLU) are studied, (CMOS) integrated circuits is related to PNPN structure formed by parasitic NPN and PNP bipolar transis-

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Transient- Induced Latchup Testing of CMOS Integrated Vol. 21, No.4, Oct 1998, pp.278-285 [8] D. Bonfert, H. Gieser, Transient Induced Latch Up

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### **Ming Dou -**

Ming-Dou Ker, To protect the radio-frequency (RF) integrated circuits from the electrostatic discharge (ESD) TRANSIENT-INDUCED LATCHUP (6)